WHAT IS CLAIMED IS:

1. A circuit for controlling the set up of a memory address, comprising:

a first latch circuit for latching a first memory address in response to a first simultaneous occurrence of a predetermined value for an output enable signal and a predetermined value for a row address strobe signal;

a second latch circuit coupled to the first latch circuit, the second latch circuit for receiving the first memory address from the first latch circuit and latching the first ~~row~~ memory address thereafter for decoding; and

wherein the first latch circuit latches a second memory address in response to a second simultaneous occurrence of the predetermined value for the output enable signal and the predetermined value for the row address strobe signal, the second simultaneous occurrence occurring while the first ~~row~~ memory address is being decoded.

2. The circuit of Claim 1, wherein each of the first latch circuit and the second latch circuit comprises:

a passgate responsive to the simultaneous occurrence of the predetermined value for the output enable signal and the predetermined value for the row address strobe signal; and

a latch coupled to the passgate.

3. The circuit of Claim 2, wherein each passgate comprises:

a p-type transistor for receiving a respective timing signal; and

an n-type transistor coupled with the p-type transistor, the n-type transistor for receiving a complement of the respective timing signal.

4. The circuit of Claim 2, wherein each latch comprises:

a first inverter having an input lead coupled to an output lead of the respective passgate; and

a second inverter having an input lead coupled to an output lead of the first inverter, the second

inverter having an output lead coupled to the input lead of the first inverter.

5. The circuit of Claim 1, further comprising a buffer coupled to the first latch circuit, the buffer for buffering an address signal conveying the first ~~row~~ memory address and the second ~~row~~ memory address.

6. The circuit of Claim 1, further comprising a timing generator circuit for generating at least one timing signal in response to the output enable signal and the row address strobe signal.

7. The circuit of Claim 1, further comprising at least one row decode circuit coupled to the second latch circuit, the row decode circuit for decoding the first and second memory addresses.

8. A method for controlling the set up of a memory address, the method comprising:

latching a first memory address in response to a first simultaneous occurrence of a predetermined value for an output enable signal and a predetermined value for a row address strobe signal;

decoding the first memory address for access to at least one memory cell corresponding to the first memory address; and

while the first memory address is being decoded, latching a second memory address in response to a second simultaneous occurrence of the predetermined value for the output enable signal and the predetermined value for the row address strobe signal.

9. The method of Claim 8, further comprising generating at least one timing signal in response to the output enable signal and the row address strobe signal.

10. The method of Claim 8, further comprising buffering an address signal which conveys the first ~~row~~ memory address and the second ~~row~~ memory address.